Modeling and Experimental Demonstration of Accelerated Self-Healing Techniques in CMOS Circuits

Mircea R. Stan, Xinfei Guo, Alec Roelke

ECE Dept., University of Virginia

*Part of this work was published at DAC2014, please refer to the paper for details.
Key Contributions

**Accelerated Self-Healing techniques**
- Control sleep conditions explicitly (e.g. higher temperatures, negative voltages)
- Proactive Accelerated Rejuvenation (control the ratio of sleep vs. active)
- Explore the *Circadian Rhythms*

**Cross-Layer Modeling**
- Consider both wearout and accelerated recovery periods
- Based on latest device level aging models
- Validated by hardware (FPGA) experiments

**Potential On-Chip Solutions**
- Negative voltage generator
- “On-Chip Heater” in other systems architectures such as Multicore
- Multiple-Critical-Path Embeddable NBTI Sensors
Aging/Wearout

• Process, Voltage, Temperature and Aging (PVTA) variations
• Parametric shift (e.g. $V_{th}$, $\mu$, $g_m$) over time
• Both Irreversible (e.g. HCl) and Reversible (e.g. BTI)
Previous Work

• Accept the variations, track and monitor them, then adapt to them (Design for worst case)
  
  T. Kim et al. [JSSC ’08], A. Cabe et al. [ISQED ’09],
  Z. Qi et al. [GLVLSI ’09], S. Kumar et al. [ASP-DAC ’09]

• Reduce/Repair aging-induced variations
  
  Stress Phase: L. Zhang et al. [ASP-DAC ’09], J. Shin, et al. [ISCA ’08]
  S. Gupta, et al. [ASP-DAC ’12][TODAES ’13]

Recovery Phase: Active Recovery (This work)

Accelerated Self-Healing
Accelerated Self-Healing

• Inspired by Biology: Sleep vs. Inactivity
  Old: Sleep = Inactivity
  New: Sleep = Active Recovery

• Sleep Conditions
  Temperature, Supply Voltages

• Proactive Recovery
  Active/Sleep Ratio

Hypothesis: Rejuvenate the chip by explicitly controlling the Ratio of Active vs. Sleep and Sleep Conditions (e.g. Higher temperatures, Negative voltage Supply)

*Source: http://gladstoneinstitutes.org/node/11312
Cross-Layer Model

- Based on Trapping/Detrapping (J. Velamala et al. [DAC ’12])
- Both stress phase and accelerated recovery phase
- Use delay change as the metric
- Fitting parameters are extracted based on measurement

\( t_1 \): Stress time; \( t_2 \): Recovery time

The total threshold voltage shift:
\[
\Delta V_{th}(t_1 + t_2) = \phi_2 (A + \log(1 + Ct_2)) + \Delta V_{th}(t_1)(1 - \frac{k + \log(1 + Ct_2)}{k + \log(1 + C(t_2 + t_1))})
\]
\[
\phi_2 \sim K_2 \exp\left(-\frac{E_0}{kT}\right)\exp\left(\frac{BV_{ddr}}{kT_{ox}}\right)
\]

The delay of a digital gate:
\[
t_d \sim \frac{C_L V_{dd}}{I_d} \propto \frac{C_L V_{dd}}{V_{dd} - V_{th}} \quad \rightarrow \quad \Delta t_d \sim \frac{\Delta V_{th}}{V_{dd} - V_{th}} \cdot t_{d0}
\]

The total delay change:
\[
\Delta T_d(t_1 + t_2) = \phi_2 t_{d0} \frac{(A + \log(1 + Ct_2))}{V_{dds}} + \Delta T_d(t_1)(1 - \frac{k + \log(1 + Ct_2)}{k + \log(1 + C(t_2 + t_1))})
\]

Delay change in one cycle (t):
\[
\Delta T_d(t) = \phi_d t_{d0} \frac{(A + \log(1 + C \frac{t}{1 + \alpha}))}{V_{dds}} + \Delta T_d\left(\frac{\alpha t}{1 + \alpha}\right)(1 - \frac{k + \log(1 + C \frac{t}{1 + \alpha})}{k + \log(1 + Ct)})
\]
Experimental Validation on FPGAs (40nm)

- Accelerated testing methodology
- Ring oscillator based test structure
- Knobs: voltage, temperature, switching activity (AC/DC) and Ratio of active and sleep time.
- 11 Test Cases

\[
T_d = \frac{1}{2f_{osc}} = \frac{1}{4C_{out} f_{ref}}
\]

Test configuration
Stress Phase Results

- **Effect of Switching Activity on aging** (T=110°C, 50% Duty Cycle)

- **Effect of temperature on performance degradation (%) for DC stress**

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>Measurement</th>
<th>Model</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>12 hours</td>
<td>24 hours</td>
</tr>
<tr>
<td>20</td>
<td>0.13%</td>
<td>0.19%</td>
</tr>
<tr>
<td>100</td>
<td>1.1%</td>
<td>1.5%</td>
</tr>
<tr>
<td>110</td>
<td>1.45%</td>
<td>2.16%</td>
</tr>
</tbody>
</table>

- Recovery is at a much slower rate → AC stress degrades the performance at a slower rate
Recovery Phase – Negative Voltage

- Vdd=-0.3V
- At two different temperature
- Even at room temperature, recovery is accelerated
Recovery Phase – High Temperature

- T=110°C
- With two different Vdd's
Model vs. Measurement

- Recovery Phase
- Model predicts the same trend
Proactive Recovery

- Scheduled Ratio of \textit{active to sleep} time $= 4$

- Summary (Recovered Percentage%)

<table>
<thead>
<tr>
<th>Case</th>
<th>Measurement(%)</th>
<th>Model(%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>20°C and 0V</td>
<td>0.66%</td>
<td>1%</td>
</tr>
<tr>
<td>20°C and -0.3V</td>
<td>16.7%</td>
<td>14.4%</td>
</tr>
<tr>
<td>110°C and 0V</td>
<td>28.7%</td>
<td>29.6%</td>
</tr>
<tr>
<td>110°C and -0.3V</td>
<td>72.4%</td>
<td>70%</td>
</tr>
</tbody>
</table>

$T=110 \, ^\circ C \quad V_{dd}=-0.3V$

Active/Sleep=4
“Circadian Rhythm” Behaviors

• Alternating phases of stress and accelerated recovery can compensate for each other, and after each recovery phase the chip can indeed start (almost) fresh.
The scheduled *active/accelerated recovery* ratio is 4 to 1.

The average performance during *active* is higher for *finer grain* active/accelerated recovery cycles.

The improvement will be *proportionally higher* as the active time increases.
**Sleep Condition:** $T = 110^\circ C, vdd = -0.3 \, V$
Accelerated Recovery “Saturation”

- Due to irreversible (permanent) part of wearout, there is a saturation once the recovery period exceeds a threshold
Proactive Periodical Accelerated Rejuvenation

• Achieve optimal average performance
• Schedule stress/accelerated recovery in the early lifetime
• The system can start (almost) fresh after each recovery period
• The irreversible wearout is “delayed” explicitly
• A wearout-adaptation strategy only needs to track rapid (reversible) wearout over a short period of time
On-chip Heating

- Multicore System

- Self-heating Blocks
  - Reconfigurable fast switching elements
    [A. Amouri et al, VTS’14] [S. Velusamy, ICCD’05]
On-chip Negative Voltages

• Widely used in memory assist circuit
  [S. Mukhopadhyay, et al., ISCA’08]
• Charge-pump based negative voltage generator
  - Embedded in a switched-cap DC-DC converter
  - Only ~5% of the total voltage regulator area
• Rejuvenate power gating header by applying a higher-than-vdd voltage
On-chip Aging Sensors - MCPENS

- MCPENS: Multiple-Critical-Path Embeddable NBTI Sensors
- Small: 200\(\mu m^2\) in a 28nm node
- Flexible: embeddable in system level design and a top-down design flow

[X. Guo et al., SELSE’15]
On-chip Aging Sensors - cont’d

• Track both aging and accelerated recovery
• Can be used together with multiple Dynamic Wearout Management (DWM) techniques
• Detect Aging-induced critical path reordering
• Can be used as triggers for Proactive Recovery

[X. Guo et al., SELSE’15]
Summary

• Accelerated self-healing techniques (Inspired by biology)
  - Sleep conditions
    • High Temperature, Negative Voltages
  - Proactive recovery (Schedule active vs. sleep)

• Modeling and Experimental Demonstration

• On-chip solutions
  - On chip heating
  - On chip negative voltage
  - On chip sensors-MCPENS
Future Work

• Exploring other sources (e.g. UV light) to accelerate recovery from wearout
• Reverse other aging mechanisms (e.g. EM)
• Develop Cross-layer optimization infrastructure
• Extend the proposed methods to emerging technologies, such as FinFET and 3DIC
Thanks!

• High-Performance Low-Power (hplp) Lab at UVa: http://hplp.ece.virginia.edu/home